REMARKS

The Applicants have filed the present Response in reply to the outstanding Official Action of December 20, 2004, and the Applicants believe the Response to be fully responsive to the Official Action for reasons set forth below in greater detail.

At the onset, the Applicants would like to note that the Applicants are submitting a substitute specification herewith. The substitute specification clarifies the spacing between several words. Furthermore, the spacing in the abstract is also clarified by the attached substitute specification. No new material was added to the specification. The substitute specification is being filed solely to clarify the spacing. As there are no amendments to the specification, there is no need for a marked up version to be filed. Additionally, the spacing between words in the claims has been modified such that the spacing is clear. Also, Figures 10-12 have been labeled as "PRIOR ART". Attached herewith are replacement sheets for Figures 10-12.

Lastly, the Examiner rejected Claims 1-11 under 35 U.S.C. § 112, second paragraph as being indefinite. Specifically, the Examiner contends that the phrase "wherein each of a plurality of sub carrier groups into which the plurality of sub-carriers are divided is assigned to each of the plurality of communication channels" as recited in Claim 1 is unclear.
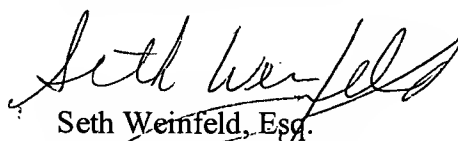
Claim 1 has been amended to clarify this limitation. More specifically, the claim has been amended to recite that the plurality of sub-carriers are divided into groups and each of said groups are assigned one group per each of the plurality of communication channels, respectively. No new matter has been added by this amendment and support

therefor can be found on page 7, line 15 through page 10, line 21 of the substitute specification.

For all the foregoing reasons, the Applicants respectfully request the Examiner to withdraw the rejections of independent Claim 1 pursuant to 35 U.S.C. § 112, second paragraph. Furthermore, the Applicants respectfully request the Examiner to withdraw the rejections of dependent Claims 2-11 based at least on their respective dependencies, whether direct or indirect, from independent Claim 1. Additionally, the Applicants respectfully request the Examiner to withdraw the objections to the specification, including the abstract, the claims, and the figures.

In conclusion, the Applicants believe that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicants respectfully request that the Examiner call the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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ORTHOGONAL FREQUENCY DIVISION MULTIPLEX MODEM CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

5   The present invention relates to an orthogonal frequency division multiplex modem circuit, and in particular, to an OFDM (Orthogonal Frequency Division Multiplex) modem circuit which transmits a plurality of different channels.

Description of the Related Art

       In recent years, the digitization of broadcasting has been promoted and an OFDM

10   system will be adopted as its modulation system.   Moreover, also in a 5-GHz-band wireless LAN (Local Area Network), the OFDM system is adopted as a modulation system.

       The OFDM system is a system that divides a transmission signal into pieces, and modulates and transmits a plenty of subcarriers respectively, and has characteristics that

15   the OFDM system has high frequency utilization efficiency and is strong on multi-path fading.

       FIG. 10 shows an example of the structure of a conventional orthogonal frequency division multiplex modem circuit.   A principle of the above-described OFDM system will be explained with using FIG. 10.   First, a transmission signal X is a signal for, for

20   example, digital high-definition television broadcasting, and consists of a 20-Mbps data signal and a 10.72-Mbps overhead (signal for error correction and synchronization control). That is, the transmission signal X is 30.72 Mbps in total.

       A 4×512-bit parallel data is generated by passing this signal through a serial/parallel converter (S/P) 101, and the data is divided every 4 bits.   Owing to this, a

25   16-value QAM (Quadrature Amplitude Modulation) baseband signal A is generated.

The 16-value QAM baseband signal A is complex data having a real part (Re) and an imaginary part (Im). Correspondence between each signal point on a complex plane and a 4-bit input signal is shown in FIG. 11.

Owing to this, 512 complex 16-value QAM signals A, each of whose symbol rates

5 is 30.72/4/512 Msps = 15 ksps, are outputted. When these 512 complex numbers are inputted into an inverse Fourier transformer (IFFT) 105, 512 sets of transformation results B are obtained. These results B are converted into a serial signal C with a parallel/serial converter (P/S) 106.

With making real parts before transformation be an I signal and making imaginary

10 parts be a Q signal, these signals are outputted to a transmitter (TX) 107 at a sample rate of 15 ksps × 512 = 7.68 Msps. The transmitter 107 performs the orthogonal modulation of the I and Q baseband signals, and outputs them from an antenna 115.

The allocation of the subcarriers in a transmitter signal is shown in FIG. 12. As shown in FIG. 12, each interval between subcarriers is equal to the symbol rate of 15 kHz

15 and the number of subcarriers is 512. Therefore, bandwidth is 15 kHz × 512 = 7.68 MHz.

Next, the structure of a receiving side will be described. In the receiving side, a high frequency signal transmitted from the transmitting side is received with an antenna 116, a receiver (RX) 108 performs an orthogonal demodulation to generate a baseband

20 signal (I, Q) D. A serial parallel converter (S/P) 109 samples this signal at the rate of 7.68 Msps respectively, and generates a parallel signal E consisting of 512 sets of I (real part) and Q (imaginary part) signals. When this signal is inputted into a discrete Fourier transformer (FFT) 110, 512 complex numbers are obtained.

This data F expresses a signal point of each corresponding sub carrier on a

25 complex plane. A corresponding 4-bit data (in the case of a 16-value QAM) is reproduced from this signal point, and is decoded into the original signal Y and outputted with a parallel/serial converter (P/S) 112.

As described above, the bit rate transmitted in the OFDM system is very high-speed, for example, 30.72 Mbps.   This is divided into many subcarriers and transmitted.   When the number of subcarriers is 512 and a modulation system is the 16-value QAM, a symbol rate per sub carrier becomes only 15 ksps.   The duration per

5   one symbol is about 67 μ sec, and this is a sufficiently large value (this is equivalent to 20 km) in comparison with the path difference of a usual multi-path.   Therefore, the OFDM system has powerful resistance to multi-path transmission.

The OFDM system is now planned with premising the utilization of each single unit such as digital television broadcast and high-speed wireless LAN equipment.

10   However, since the OFDM system has a feature of being essentially strong on the multi-path transmission, this feature is attractive also in other mobile communications.

Therefore, as a natural conclusion, it can be thought that demands for using the OFDM system also for mobile communications come out.   However, since the OFDM system realizes vast transmission capacity as a whole by using hundreds of subcarriers, it

15   is not allowed to use this monopolistically by one kind of mobile communication.

Therefore, it is possible to transmit various communications, such as digital TV, wireless LAN, the Internet, and cellular phones, via one OFDM line.   The plural kinds of communication signals have different bit rates respectively, and their necessary transmission quality (QoS: Quality of Service) are different according to informational

20   types.

That is, there are various transmission rates (for example, 28.8 kbps, 1.44 Mbps, and 10 Mbps) in data communication, and, an error rate not higher than 10E-6 is required. On the other hand, in speech communication such as a telephone, a transmission rate is 13 kbps or the like, and the error rate of 10E-3 is regarded as sufficient quality.

25   SUMMARY OF THE INVENTION

Then, an object of the present invention is to solve the above-described troubles, and to provide an orthogonal frequency division multiplex modem circuit which can

multiplex signals, whose bit rates and QoS are different from one another, and can transmit the signals via one OFDM line.

An orthogonal frequency division multiplex modem circuit according to the present invention is an orthogonal frequency division multiplex modem circuit that uses a plurality of subcarriers for communication, and transmits and receives a plurality of communication channels. In the circuit, each of a plurality of sub carrier groups into which the plurality of subcarriers is divided is assigned to each of the plurality of communication channels.

That is, the orthogonal frequency division multiplex modem circuit according to the present invention provides a method for multiplexing and transmitting a plurality of communication channels whose bit rates and QoS (Quality of Service) are different from one another, via one OFDM (Orthogonal Frequency Division Multiplex) line.

In order to achieve this, a first orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that performing communications with using a plurality of subcarriers, dividing the plurality of subcarriers into a plurality of groups in an OFDM system which transmits and receives a plurality of communication channels, and assigning the sub carrier groups to the plurality of communication channels respectively.

A second orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that the assignment of sub carrier groups to respective communication channel is adaptively performed.

A third orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that a modulation system given to each of the sub carrier groups is changed according to the QoS (Quality of Service) needed for a corresponding communication channel.

A fourth orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that means for randomizing the alignment of the

respective subcarriers on a frequency axis is included in a transmitting side, and that means for de-randomizing the alignment is included in a receiving side.

A fifth orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that all subcarriers are assigned to a single channel as required, while communication of other channels is stopped.

A sixth orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that the changeable modulation system that is described above uses phase modulation such as BPSK (Binary Phase Shift Keying), QPSK (Quadrature Phase Shift Keying), and QAM (Quadrature Amplitude Modulation), and a symbol point on a phase plane is changed according to the QoS.

A seventh orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that, since it is desirable for the transmitted power of each sub carrier to be uniform, a peak value of each modulation symbol is determined so that the transmission power of the respective subcarriers may become the same irrespective of the modulation system.

An eighth orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that the processing for randomizing positions of respective subcarriers is updated every symbol as means for preventing the suppression of a specific sub carrier caused by frequency-selective fading.

A ninth orthogonal frequency division multiplex modem circuit according to the present invention is characterized in comprising means for determining a randomization pattern every symbol and transmitting the randomization pattern every symbol to the receiving side is included in the transmitting side, and means for synchronizing transmission and reception of the randomization pattern is included.

A tenth orthogonal frequency division multiplex modem circuit according to the present invention is characterized in that the orthogonal frequency division multiplex modem circuit comprises means for determining a randomization pattern every symbol and transmitting the randomization pattern every symbol to the receiving side is included

in the transmitting side, and that a predetermined communication channel and a sub carrier corresponding to it are assigned as the means for synchronizing transmission and reception of the randomization pattern.

An eleventh orthogonal frequency division multiplex modem circuit according to

5   the present invention is characterized in that a predetermined communication channel and a sub carrier corresponding thereto is excluded from randomization process.

Owing to the above-described structure and processing operation, the orthogonal frequency division multiplex modem circuits of the present invention can transmit communication channels whose bit rates and QoS are different from one another with

10   using one OFDM line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the structure of an orthogonal frequency division multiplex modem circuit according to an embodiment of the present invention;

FIG. 2 is a block diagram showing a structural example of the serial/parallel

15   converter shown in FIG. 1;

FIG. 3 is a block diagram showing a structural example of the serial/parallel converter shown in FIG. 1;

FIG. 4 is a diagram for explaining the randomizer of FIG. 1;

FIG. 5 is a diagram for explaining the de-randomizer of FIG. 1;

20   FIG. 6 is a time chart showing the operation of the serial/parallel converter of FIG. 2;

FIG. 7 is a time chart showing the operation of the serial/parallel converter of FIG. 3;

FIG. 8 is a graph showing symbol points on a complex plane;

25   FIG. 9 is a block diagram showing the structure of an orthogonal frequency division multiplex modem circuit according to another embodiments of the present invention;

FIG. 10 is a block diagram showing the structure of a orthogonal frequency division multiplex modem circuit according to a conventional example;

FIG. 11 is a graph showing correspondence of respective signal points on a complex plane, and 4-bit input signals; and

5   FIG. 12 is a diagram showing the allocation of subcarriers in a transmitter signal.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Next, embodiments of the present invention will be described with reference to drawings.   FIG. 1 is a block diagram showing the structure of an orthogonal frequency division multiplex modem circuit according to an embodiment of the present invention.

10   In FIG. 1, the orthogonal frequency division multiplex modem circuit according to this embodiment of the present invention comprises a transmitting side consisting of serial/parallel converters (S/P) 101, 102, and 103, a randomizer 104, a discrete inverse Fourier transformer (IFFT) 105, a parallel/serial converter (P/S) 106, and a transmitter (TX) 107, and a receiving side consisting of a receiver (RX) 108, a serial/parallel converter

15   (S/P) 109, a discrete Fourier transformer (FFT) 110, a de-randomizer 111, and parallel/serial converters (P/S) 112, 113, and 114.

FIG. 2 is a block diagram showing a structural example of the serial/parallel converter 101 shown in FIG. 1.   In FIG. 2, the serial/parallel converter 101 consists of a shift register 601 and 16-value QAM (Quadrature Amplitude Modulation) generating

20   circuits 602, 603, 604, and 605.

FIG. 3 is a block diagram showing a structural example of the serial/parallel converter 102 shown in FIG. 1.   In FIG. 3, the serial/parallel converter 102 consists of a shift register 701 and QPSK (Quadrature Phase Shift Keying) generating circuits 702, 703, 704, and 705.

25   FIG. 4 is a drawing for explaining the randomizer 104 shown in FIG. 1, and FIG. 5 is a drawing for explaining the de-randomizer 111 shown in FIG. 1.   FIG. 6 is a time chart showing the operation of the serial/parallel converter 101 shown in FIG. 2, and FIG.

7 is a time chart showing the operation of the serial/parallel converter 102 shown in FIG. 3. In addition, FIG. 8 is a graph showing symbol points on a complex plane. With reference to these FIGS. 1 to 8, the operation of the orthogonal frequency division multiplex modem circuit according to this embodiment of the present invention will be described.

5   Differently from the conventional example of the orthogonal frequency division multiplex modem circuit shown in FIG. 10, the orthogonal frequency division multiplex modem circuit according to this embodiment of the present invention has a plurality of data inputs X1, X2, ..., Xn in the transmitting side, and has a plurality of data outputs Y1, Y2, ..., Yn, corresponding thereto, also in the receiving side.

10   The input signals X1, X2, ..., Xn are converted into a complex parallel signal A with the serial/parallel converters 101, 102, and 103 respectively. For example, the input signal X1 is inputted at the bit rate of 240 kbps. If the QoS of the input signal X1 is a middle degree, four subcarriers are assigned, and an output of the serial/parallel converter 101 becomes four complex numbers (it corresponded to four subcarriers) at 15 ksps in the

15   case that a modulation system is the 16-value QAM.

In the serial/parallel converter 101 generating the 16-value QAM, as shown in FIG. 2, data is inputted into the shift register 601 driven by a clock having a frequency equal to the data rate. The 4-bit parallel outputs of the shift register 601 are a group at a time, and are inputted into the 16-value QAM generating circuits 602,603,604,605 respectively to be

20   incorporated with a clock (Symbol CLOCK) equal to the symbol rate.

According to each incorporated 4-bit value, a symbol point on a complex plane as shown in FIG. 11 is chosen, and each real part (Re) and imaginary part (Im) are outputted. FIG. 6 shows a timing chart of the operation.

When the bit rate is 120 kbps and QoS is high, four subcarriers are assigned to the

25   input signal X2 and the QPSK with a low error rate is used as a modulation system. In this case, an output of the serial/parallel converter 102 also becomes four complex numbers at 15 kbps (it corresponded to four subcarriers).

In the serial/parallel converter 102, as shown in FIG. 3, data is inputted into the shift register 701 driven with a clock having a frequency equal to a data rate.   An parallel output of the shift register 701 is set every 2 bits, and is inputted into the QPSK generating circuits 702, 703, 704, and 705 respectively to be incorporated with a clock (Symbol

5   CLOCK) equal to a symbol rate.

According to the incorporated value of 2 bits, a symbol point on a complex plane as shown in FIG. 8 is chosen, and each real part (Re) and an imaginary part (Im) are outputted.   A timing chart of the operation is shown in FIG. 7.

Similarly, if the QoS of the input signal Xn is not so high and its bit rate is 90 kbps,

10   a sub carrier is assigned.   In addition, when a modulation system is a 64-value QAM, an output of the serial/parallel converter 103 also becomes one complex number at 15 ksps (it corresponded to one sub carrier).

As described above, an adequate modulation system and the number of subcarriers to be assigned can be determined from the bit rate and QoS, and the symbol rates of all

15   subcarriers can be set to the same rate, 15 kHz.

As described above, subcarriers and a modulation system are assigned for every communication channel, and 512 complex data symbols (at the symbol rate of 15 kbps) in total are obtained.   In this case, if a communication channel is insufficient and a sub carrier is surplus, the sub carrier can be made not to be modulated, that is, to be a complex

20   number (0+j0).

Thus, the sequence of the alignment of 512 pieces of parallel complex data obtained in this manner is replaced by the randomizer 104.   This operation is performed per symbol.   The randomizer 104, as shown in FIG. 4, replaces the sequence every symbol with a control signal (for example, 8 bits).   If the control signal is 8 bits, 256

25   kinds of replacement can be performed.   In FIG. 4, although the input signals X510 and X511 are connected to Y510 and Y511 as it is, this supposes the control channel.

The control channel is to transmit symbol synchronization and information about a randomization pattern to the receiving side. Hence, it facilitates an initial access to transmit it as it is without performing randomization.

The discrete inverse Fourier transformer 105 processes 512 pieces of randomized
5   parallel complex data A' to obtain 512 sets of I and Q parallel data B. The parallel/serial converter 106 converts this result into a serial signal C. The parallel/serial converter 106 makes a real part before transformation be an I signal, makes an imaginary part be a Q signal, and outputs them to the transmitter 107 at the sample rate of 15 ksps $\times$ 512 = 7.68 Msps. The transmitter 107 performs the orthogonal modulation of the I and Q baseband
10   signals, and outputs them from the antenna 115.

FIG. 12 shows the allocation of the subcarriers in a transmitter signal. As shown in FIG. 12, each interval between subcarriers is equal to 15 kHz that is the symbol rate, and the number of subcarriers is 512. Therefore, bandwidth is 15 kHz $\times$ 512 = 7.68 MHz.

Next, the operation of the receiving side will be described. The receiving side
15   receives the high frequency signal transmitted from the transmitting side with the antenna 116, and performs orthogonal demodulation with the receiver 108 to generate a baseband signal (I and Q) D. The receiving side samples this at the rate of 7.68 Msps with the serial/parallel converter 109 respectively to generate a parallel signal E that consists of 512 sets of I (real part) and Q (imaginary part) signals. The discrete Fourier transformer 110
20   receives this signal to output 512 complex numbers.

These data F' express signal points of corresponding subcarriers on a complex plane. The de-randomizer 111 receives this result, and restores the sequence of the subcarriers that is changed in the randomizer 104.

The de-randomizer 111 replaces the sequence per symbol with the control signal
25   (for example, 8 bits), as shown in FIG. 5. If the control signal is 8 bits, 256 kinds of replacement can be performed. In FIG. 5, although the input signals Y510 and Y511 are connected to X510 and X511 as it is, this supposes the control channel.

The control channel is to transmit symbol synchronization and information about a randomization pattern to the receiving side. Hence, it facilitates an initial access to transmit them as they are without performing randomization.

The result F of the de-randomization expresses signal points of corresponding

5 subcarriers on a complex plane. The corresponding bit data is restored from these signal points and the modulation systems of respective subcarriers, and is decoded and outputted to the original signals Y1 and Y2, ..., Yn with the parallel/serial converters 112, 113, and 114.

Thus, it becomes possible by performing the above processing operation to

10 transmit a plurality of communication channels, whose bit rates and QoS are different from one another, via one OFDM line.

FIG. 9 is a block diagram showing the structure of an orthogonal frequency division multiplex modem circuit according to another embodiment of the present invention. In FIG. 9, the structure of the orthogonal frequency division multiplex modem

15 circuit with a single channel is shown.

That is, the orthogonal frequency division multiplex modem circuit according to this embodiment of the present invention comprises a transmitting side consisting of a serial/parallel converter (S/P) 101, a randomizer 104, a discrete inverse Fourier transformer (IFFT) 105, a parallel/serial converter (P/S) 106, and a transmitter (TX) 107,

20 and a receiving side consisting of a receiver (RX) 108, a serial/parallel converter (S/P) 109, a discrete Fourier transformer (FFT) 110, a de-randomizer 111, and a parallel/serial converter (P/S) 112.

The orthogonal frequency division multiplex modem circuit according to embodiment of the present invention is primarily intended to transmit a plurality of

25 communication channels with different bit rates and QoS via one OFDM line. However, with depending on the case, only one communication channel can be passed preferentially.

For example, when it is necessary to relay digital Hi-Vision TV broadcasting, it becomes necessary to assign all subcarriers to this. In such a case, it is also conceivable

to stop other communication channels with lower priorities temporarily and to use all subcarriers for one preference channel. Hence, the orthogonal frequency division multiplex modem circuit according to this embodiment of the present invention has the above-described structure.

5   Thus, the present invention includes also adaptively determining the assignment of subcarriers and modulation systems according to the priorities, bit rates, and QoS of communication channels.

   Moreover, it is not desirable that difference of mean signal power arises between the subcarriers whose modulation systems differ. The present invention includes also

10 making the mean signal power of all subcarriers uniform by adjusting peak values of symbols.

   As described above, the present invention has an advantage that, the orthogonal frequency division multiplex modem circuit which uses a plurality of subcarriers for communication, and transmits and receives a plurality of communication channels can

15 multiplex and transmit signals, whose bit rates and QoS are different from one another, via one OFDM line by assigning each of sub carrier groups, into which the plurality of subcarriers is divided, to each of the plurality of communication channels.

20

ABSTRACT OF THE DISCLOSURE

To provide an orthogonal frequency division multiplex modem circuit which can multiplex signals, whose bit rates and QoS are different from one another, and can transmit the signals via one OFDM line.   A serial/parallel converter converts input signals into a

5   complex parallel signal respectively, and a sub carrier and a modulation system are assigned every communication channel.   A randomizer changes the alignment sequence of the signal, a discrete inverse Fourier transformer processes the signal, a parallel/serial converter converts the signal into a serial signal, and a transmitter performs the orthogonal modulation of the signal to output the signal from an antenna.   A receiver performs

10   orthogonal demodulation of the signal received with an antenna, a serial/parallel converter converts the signal into a parallel signal, and a discrete Fourier transformer processes the parallel signal.   In addition, a de-randomizer restores the alignment sequence of the subcarriers into the original condition, and a parallel/serial converter decodes and outputs the signal.